UNITED STATES PATENT APPLICATION

FOR

HIGH-VOLTAGE SWITCHES IN SINGLE-WELL CMOS PROCESSES

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SPECIFICATION

TITLE OF INVENTION

HIGH-VOLTAGE SWITCHES IN SINGLE-WELL CMOS PROCESSES

STATEMENT OF RELATED APPLICATIONS

[0001] This application claims the benefit of United States Provisional Patent Application Serial No. 60/500,460 filed September 5, 2003 and having the same title and inventors and being commonly assigned herewith. This application is also related to United States Patent Application Serial Nos. 10/______, 10/______ and 10/______, all entitled "Rewriteable Electronic Fuses" and filed on even date herewith, commonly assigned and in the name of inventors Christopher J. Diorio, Frederic Bernard and Todd E. Humes (Attorney Docket Nos. IMPJ-0027A, IMPJ-0027B and IMPJ-0027C, respectively).

FIELD OF THE INVENTION

[0002] The present invention is directed to high-voltage switches implemented in single-well CMOS (complementary metal oxide semiconductor) processes.

BACKGROUND OF THE INVENTION

[0003] Certain types of nonvolatile memory devices, circuits employing floating-gate devices, high-voltage drivers and other circuits fabricated in logic CMOS require relatively high voltages (e.g., 10 volts in a 3.3 volt CMOS process). For example, in nonvolatile memory devices high voltages are often used to by circuits that program and

erase information stored on the floating gates, and on-chip charge pumps are generally used to generate these high voltages. In all these circuits, switches are required to selectively apply the high voltages to specific circuit elements.

[0004] The only silicon structure in generic n-well CMOS processes (where "generic" means that a process lacks specialized structures, such as for high-voltage devices, and n-well is the most common process type in the industry) that can handle voltages significantly greater than the logic supply voltage is an n-well. This limitation means that there are only three types of high-voltage structures that can be built in such a generic n-well CMOS process: (1) an nFET (n-channel Field Effect Transistor) that has an n-well for its drain and/or source and examples of which include the Lateral-Diffused Metal-Oxide Semiconductor nFET (LDMOS nFET) and Drain Extended MOS nFET (DEMOS nFET); (2) well resistors or well wires, where the well is used as a conductive element that can tolerate high voltages; and (3) pFETs (p-channel Field Effect Transistors) in an n-well, where the n-well itself can be at a high voltage relative to the substrate. Because a single pFET cannot normally handle drain-to-source voltages much larger than the rated supply voltage for a given process (e.g., not much more than 3.3V for a 3.3V CMOS process), it is common to cascode a plurality of pFETs (i.e., put two or more in series) in one or more n-wells, in order to handle such high voltages. Note that these same three basic devices can be fabricated in p-well CMOS processes, with p replaced by n (and *vice versa*), and with positive voltages replaced by negative voltages (and *vice versa*).

[0005] Switch circuits which can tolerate a high-voltage supply and can generate and use intermediate voltages, as well as generate high-voltage drive signals from low-voltage logic-gate-level signals, all while minimizing power consumption, are highly desired.

BRIEF DESCRIPTION OF THE INVENTION

[0006] Circuits are provided for high-voltage switching in low-voltage CMOS processes. In a first aspect of the invention, a switch circuit for providing a switched high-voltage signal in response to an input logic-level state includes: a first pFET having a source, drain, well and gate terminal, the source and well coupled to a source of a high-voltage signal (the source and well do not have to be coupled to the same source of a high-voltage signal), the drain coupled to an intermediate node and the gate coupled to a control node; a second pFET having a source, drain, well and gate terminal, the source and well coupled to the intermediate node, the drain coupled to a voltage output node and providing the switched high-voltage signal, the gate coupled to a source of a first Intermediate-Voltage, the first Intermediate-Voltage being intermediate the high-voltage and a ground; a diode having its anode coupled to a source of a second Intermediate-Voltage (which may be the first Intermediate-Voltage), the second Intermediate-Voltage being intermediate the High-Voltage and the ground, and its cathode coupled to the intermediate node; and a High-Voltage MOS nFET having a source, drain and gate terminal, the source coupled to the ground, the drain coupled to the voltage output node and the gate coupled to a source of the input logic-level state.

[0007] In a second aspect of the invention the high-voltage MOS nFET is cascoded with one or more additional nFETs to reduce the voltage stress on the various circuit components and in that manner a switch circuit for providing a switched high-voltage signal in response to an input logic-level state includes: a first pFET having a source,

drain, well and gate terminal, the source and well coupled to a source of a high-voltage signal, the drain coupled to a first intermediate node and the gate coupled to a control node; a second pFET having a source, drain, well and gate terminal, the source and well coupled to the first intermediate node, the drain coupled to a voltage output node and providing the switched high-voltage signal, the gate coupled to a source of a first Intermediate-Voltage, the first Intermediate-Voltage being intermediate the high-voltage and a ground; a first diode having its anode coupled to a source of a second Intermediate-Voltage (which may be the first Intermediate-Voltage), the second Intermediate-Voltage being intermediate the High-Voltage and the ground, and its cathode coupled to the first intermediate node; a MOS nFET having a source, drain and gate terminal, the source coupled to the ground, the drain coupled to a second intermediate node and the gate coupled to a source of the input logic-level state; and a high-voltage MOS nFET having a source, drain and gate terminal, the source coupled to the drain of the MOS nFET, the drain coupled to the voltage output node and the gate coupled to a source of Vdd, the Vdd being a voltage between the Intermediate-Voltages and the ground.

[0008] In accordance with various other aspects of the invention: (1) the first and second Intermediate-Voltages may be the same or essentially the same, e.g., sourced from the same voltage supply or from supplies set to provide essentially the same voltages; (2) the high-voltage nFET(s) may comprise a drain region having an n+ region disposed within an n- well in the p- bulk of a semiconductor substrate; (3) various forms of a pull-up circuit may be coupled to the control node to raise it to the high-voltage; (4) a

capacitor may be coupled between the control node and a logic-level input node; (5) the various diodes may be formed of nFET MOS devices and/or pFET MOS devices, or they may be n-well diodes, as desired; and (6) the control node may be coupled to a latch-type circuit with or without precharge capability.

[0009] In yet another aspect of the present invention a circuit for providing a differential switched high-voltage signal in response to a pair of complementary Reset-Set input logic-level signals, includes: a first and a second pFET each having a source, drain, well and gate terminal, the source and well of each coupled to a source of a high-voltage signal, the drain of the second pFET coupled to a first intermediate node and its gate coupled to a second intermediate node, the drain of the first pFET coupled to the second intermediate node and its gate coupled to the first intermediate node; a first circuit portion responsive to the Set signal and a Preset signal coupled to the first intermediate node to enable assertion of the Set signal to the first intermediate node when the Preset signal is asserted; a second circuit portion responsive to the Reset signal and the Preset signal coupled to the second intermediate node to enable assertion of the Reset signal to the second intermediate node when the Preset signal is asserted; a third and fourth pFET, said third pFET having its source coupled to the first intermediate node, its drain coupled to a first of two complementary switched voltage output nodes and its gate coupled to an intermediate-voltage supply, and said fourth pFET having its source coupled to the second intermediate node, its drain coupled to the second of two complementary switched voltage output nodes and its gate coupled to the intermediate-voltage supply; and a first and a second high-voltage nFET, said first high-voltage nFET

having its drain coupled to the first of two complementary switched voltage output nodes, its gate coupled to a Vdd supply, and its source coupled to GND through a first transistor responsive to the Reset signal, said second high-voltage nFET having its drain coupled to the second of two complementary switched voltage output nodes, its gate coupled to the Vdd supply, and its source coupled to GND through a second transistor responsive to the Set signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The accompanying drawings, which are incorporated into and constitute a part of this specification, illustrate one or more embodiments of the present invention and, together with the detailed description, serve to explain the principles and implementations of the invention.

[0011] In the drawings:

FIG. 1 is an electrical schematic diagram of a high-voltage nFET switch circuit with a cascaded pFET stack on top and a current-mirror driver in accordance with the prior art.

FIG. 2 is a side elevational cross-sectional view of a single high-voltage LDMOS nFET for high-voltage use in accordance with the prior art.

FIG. 3 is an electrical schematic diagram of a first modification of the switch circuit of FIG. 1 in accordance with an embodiment of the present invention.

FIG. 4 is an electrical schematic diagram of a second modification of the switch circuit of FIG. 1 in accordance with another embodiment of the present invention.

FIG. 5 is an electrical schematic diagram of a third modification of the switch circuit of FIG. 1 in accordance with another embodiment of the present invention.

FIG. 6 is an electrical schematic diagram of a fourth modification of the switch circuit of FIG. 1 in accordance with yet another embodiment of the present invention.

FIG. 7 is an electrical schematic diagram showing an implementation of the high-voltage capacitor of FIG. 2 using two MOSFETs. Although drawn with pFETs, the actual implementation could use pFETs, nFETs, MOSCAPs, or other MOS devices as are known to those of ordinary skill in the art.

FIG. 8 is an electrical schematic diagram showing an implementation of the high-voltage capacitor of FIG. 3 using a metal-insulator-metal (MIM) capacitor or a polysilicon-insulator-polysilicon (PIP) capacitor.

FIG. 9 is an electrical schematic diagram showing an implementation of the high-voltage capacitor of FIG. 3 using a fringe capacitor.

FIG. 10 is an electrical schematic diagram of two possible implementations of the diodes featured in FIGS. 3, 4, 5, 6, 14A, 14B, 15, 16, and 17.

FIG. 11 is a side elevational cross-sectional view of a pn-junction diode as may be used for the diodes featured in FIGS. 3, 4, 5, 6, 14A, 14B, 15, 16, and 17.

FIG. 12 is an alternative implementation of the high-voltage nFET featured in FIGS. 3, 4, 5, 6, 13, 14A, 14B, 15, 16, 17, 18.

FIG. 13 is an electrical schematic diagram of a fifth modification of the switch circuit of FIG. 1 in accordance with yet another embodiment of the present invention.

FIG. 14A is an electrical schematic diagram of a sixth modification of the switch circuit of FIG. 1 in accordance with yet another embodiment of the present invention.

FIG. 14B is a modification of FIG. 14A adding diode-coupled transistors D3 and D4 to limit the voltage across the high voltage nFETs.

FIG. 15 is an electrical schematic diagram of a seventh modification of the switch circuit of FIG. 1 in accordance with yet another embodiment of the present invention.

FIG. 16 is an electrical schematic diagram of an eighth modification of the switch circuit of FIG. 1 in accordance with yet another embodiment of the present invention.

FIG. 17 is an electrical schematic diagram of a ninth modification of the switch circuit of FIG. 1 in accordance with yet another embodiment of the present invention.

FIG. 18 is an electrical schematic diagram of a tenth modification of the switch circuit of FIG. 1 in accordance with yet another embodiment of the present invention.

DETAILED DESCRIPTION

[0012] Embodiments of the present invention are described herein in the context of high-voltage switch circuits implemented in single-well CMOS processes. Those of ordinary skill in the art will realize that the following detailed description of the present invention is illustrative only and is not intended to be in any way limiting. Other embodiments of the present invention will readily suggest themselves to such skilled persons having the benefit of this disclosure. Reference will now be made in detail to implementations of the present invention as illustrated in the accompanying drawings. Where appropriate, the same reference indicators will be used throughout the drawings and the following detailed description to refer to the same or similar parts.

[0013] In the interest of clarity, not all of the routine features of the implementations described herein are shown and described. It will, of course, be appreciated that in the development of any such actual implementation, numerous implementation-specific decisions must be made in order to achieve the developer's specific goals, such as compliance with application- and business-related constraints, and that these specific goals will vary from one implementation to another and from one developer to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking of engineering for those of ordinary skill in the art having the benefit of this disclosure.

[0014] As used herein, the symbol n+ indicates an n-doped semiconductor material typically having a doping level of n-type dopants on the order of 10^{21} atoms per cubic

centimeter. The symbol n- indicates an n-doped semiconductor material typically having a doping level on the order of 10^{17} atoms per cubic centimeter. The symbol p+ indicates a p-doped semiconductor material typically having a doping level of p-type dopants on the order of 10^{21} atoms per cubic centimeter. The symbol p- indicates a p-doped semiconductor material typically having a doping level on the order of 10^{17} atoms per cubic centimeter. Those of ordinary skill in the art will now realize that the devices described herein may be formed on a conventional semiconductor substrate or they may as easily be formed as a thin film transistor (TFT) above the substrate, or in silicon on an insulator (SOI) such as glass (SOG), sapphire (SOS), or other substrates as known to those of ordinary skill in the art. Such persons of ordinary skill in the art will now also realize that a range of doping concentrations around those described above will also work. Essentially, any process capable of forming pFETs and nFETs will work. Doped regions may be diffusions or they may be implanted.

[0015] Turning now to the figures, FIG. 1 is an electrical schematic diagram illustrating an electrical switch circuit 10. Circuit 10 includes a high-voltage (capable of handling more than Vdd across its drain-source) nFET N1 which may be of the LDMOS type, DEMOS type or any other suitable type. The circuit symbol for nFET N1 includes a square symbol 11 surrounding the drain of nFET N1 which denotes a drain comprising an n+ region disposed in an n- well for tolerating higher voltages. This symbol will be used throughout this disclosure to indicate a high-voltage nFET. Circuit block 12 is a cascoded pFET stack comprising pFETs P2 and P3 with intermediate node IN disposed between them and coupled to the drain of pFET P2 and the source of pFET P3. Current

mirror driver circuit block 13 acts as a pull-up to provide high-voltage source HV to control node 14 (shown as signal CTRL on control node 14).

[0016] Circuit 10 operates as follows. Logic input LI1 (working within the voltage range of GND – Vdd) is applied to the gate of high-voltage nFET N2. If LI1 is high then transistor N2 will conduct, if not, it will not. If it conducts, it will pull control node 14 down from a high-voltage causing pFET P2 to conduct from a high-voltage supply HV (which may be the same as the HV supply applied to the source of pFET P1, but it need not be the same). With pFET P2 conducting, intermediate node IN is brought up to HV. The pFET P3 is forced on by Intermediate-Voltage (IV) to form a cascode with pFET P2. Since logic input LI2 is in opposite phase with LI1, when LI1 is high and N2 is conducting, LI2 is low and N1 is not conducting. In this way, Vout is high and provides the output of the high-voltage supply. Switching the state of LI1 and LI2 forces Vout to be low because control node 14 stays high (pulled high by current mirror driver 13) which turns off pFET P2. Since LI2 is now high, Vout is brought to ground (GND) through transistor N1 since it is conducting. Note that throughout this disclosure, where multiple sources of high-voltage (HV) are required, they may be from the same source, or they may be from different sources at different voltage levels, if appropriate and desirable. The same applies for sources of Intermediate-Voltages (which typically have a magnitude between HV and Vdd). Sources of HV or IV may be obtained from conventional charge-pump circuits operating off of the GND-Vdd supply as is well known to those of ordinary skill in the art and are, accordingly, not shown or discussed further herein.

[0017] There are some issues with circuit 10. First, the current mirror draws continuous power from the HV supply whenever HV nFET N2 is turned on, which is not desirable for low-power applications. Second, during switching operations, it is possible to see more than HV/2 volts across pFET P3 which may present reliability problems. Accordingly, several embodiments of the present invention involve alternative ways to drive the signal CNTL on the control node 14 of the circuit of FIG. 1 (and modifications thereof). Several embodiments also address the cascoded pFET circuit 12 and ways to modify it to make it more robust.

[0018] FIG. 2 is a side elevational cross-sectional view of a single high-voltage LDMOS nFET 20 for high-voltage use in accordance with the prior art. Transistor 20 is fabricated on a p- substrate 22 and includes p+ region 24 that provides a substrate contact and a means to ground the substrate 22. A first n- well 26 and a first n+ diffusion 28 are provided. Within first n- well 26 is an n+ region 30 which, together with region 26, serves as the drain of transistor 20. A channel 32 exists between first n- well 26 and first n+ diffusion 28. An insulation layer 34 is provided over channel 32 to insulate a gate 36 from the substrate 22. The insulation layer 34 may be any appropriate insulator as known to those of ordinary skill in the art, such as a gate oxide which may grown or deposited. Gate 36 may comprise highly doped polycrystalline silicon, a metal, or other conductive materials known to those of ordinary skill in the art.

[0019] FIG. 3 is an electrical schematic diagram of a first modification 38 of the switch circuit of FIG. 1 in accordance with an embodiment of the present invention. In

accordance with the embodiment illustrated in FIG. 3, a simple charge-based current mirror 16 uses a high-voltage capacitor C1 to couple charge to the control node 14 and thereby control the switch portion 39 of the circuit. In accordance with this embodiment of the invention, the Vout node doesn't have to remain high for extended periods of time (i.e., Vout is pulsed high), so the CNTL signal on control node 14 can be pulled down through capacitor C1 with good switching action at the Vout node. The capacitor C1 may be implemented as a polysilicon-insulator-polysilicon (PIP) capacitor or a metal-insulator-metal (MIM) capacitor as illustrated in FIG. 8, a fringe capacitor as illustrated in FIG. 9, or using the gate-to-channel capacitance of MOSFETs. Typically a pair of MOSFETs rather than a single MOSFET will be used, to increase the gate-oxide breakdown voltage above that of a single MOSFET, such as a pair of p-channel MOSFETs (e.g., pFETs in n-wells as illustrated in FIG. 7). When using series-connected MOSFETs, the individual MOSFETs in each pair do not necessarily have the same sizes and/or the same values, and each MOSFET in the pair can be constructed from a plurality of smaller MOSFETs connected in parallel. Turning to the switch portion 39 of the circuit, Diode D1 ensures that, when Vout is at a low voltage, the potential difference between the high-voltage supply and this low output voltage is shared across the drain–source junctions of cascoded pFETs P2 and P3. Diode D1 clamps the voltage at node IN to a value near the Intermediate-Voltage (IV)minus Vf, where Vf is diode D1's forward turn-on voltage drop. Alternatively, instead of coupling diode D1's anode to IV, a separate Intermediate-Voltage supply could be used to bias the anode of D1.

[0020] FIG. 4 is an electrical schematic diagram of a second modification 42 of the switch circuit of FIG. 1 in accordance with another embodiment of the present invention. In accordance with this embodiment of the invention a single pFET P1 is added to ensure that the CNTL signal on control node 14 is pulled up to HV when the Vout node is low. P1 sources a continuous small current typically in the range of about 100pA to about 100nA, or can be switched on and off where in the "on" state it typically sources a current in a range of about 100pA to about 100μA. In either case the purpose is to pull CNTL to the high-voltage supply and so turn off pFET P2 and eliminate static power consumption when Vout is low. In other respects, the circuit 42 is similar to circuit 38 of FIG. 3 and the switch portion 43 of circuit 42 operates in the same manner as the switch portion 39 of circuit 38 in FIG. 3.

[0021] FIG. 5 is an electrical schematic diagram of a third modification 44 of the switch circuit of FIG. 1 in accordance with another embodiment of the present invention. In accordance with this embodiment, a high-voltage RS (reset-set) latch circuit 46 is used for driving CNTL on control node 14 to, in turn, control the switch portion 45 of the circuit (which operates in the same manner as switch portion 39 of circuit 38 in FIG. 3. LI (coupled to N1's gate), Set and Reset are low voltage logic signals that typically swing from GND to Vdd. Set and Reset are complementary. LI is tied to Reset. HV latch 46 operates as follows. If the Reset input at the gate of HV nFET N2 is high and the corresponding Set input at the gate of HV nFET N3 is low, N2 is on, N3 is off, node A is pulled low because N2 is on and this turns on P5. Since N3 is off, the HV applied to the source of P5 brings the control node 14 up to HV. Note that in this case the HV latch 46

consumes static power from the Intermediate-Voltage supply (IV1) flowing through D2 and N2 to GND, but not from the high-voltage supply (HV). Similarly, if the Reset input at the gate of N2 is low and the Set input at the gate of N3 is high, then N2 is OFF and N3 is on (conducting) which tends to bring control node 14 down to IV1 less the voltage drop through diode D3. Again, static power is consumed from the IV1 power supply.

[0022] FIG. 6 is an electrical schematic diagram of a fourth modification 48 of the switch circuit of FIG. 1 in accordance with yet another embodiment of the present invention. In accordance with this embodiment, two currents, the first sourced by pFET P1 in pull-up circuit 50 and the second, larger than the first and sunk by high-voltage nFET N2, are used to drive the signal CNTL on control node 14. N2 is a high-voltage nFET which may be of the LDMOS type, the DEMOS type or any other suitable high-voltage nFET type as discussed above. This circuit consumes a small amount of power from the high-voltage supply when the output voltage node Vout is high, because N2 is turned on and must overcome the small current sourced by pFET P1. In the more common situation, when the output voltage node Vout is low, this circuit does not consume any power from the high-voltage supply because N2 is turned off, the control node 14 pulls up to the high-voltage supply HV, and there is no path from the high-voltage supply to ground. In the high-voltage switch portion 49 of the circuit 48 slight differences are illustrated over switch portion 39 of circuit 38 in FIG. 3. As shown, diode D2 and pFET P3 may be connected to different Intermediate-Voltages (IV2, IV3) rather than to a single common Intermediate-Voltage (IV); the ability to use such separate supplies applies to all embodiments of the present invention, as will now be apparent to

those skilled in the art (e.g., the node supplied with IV-2 may be coupled to the IV-3 supply and the IV-2 supply omitted (or *vice versa*).

[0023] FIG. 7 is an electrical schematic diagram of a high-voltage capacitor 51 realized with two p-channel MOSFETs M1 and M2. A bias circuit may be used to set a voltage on the n-well that is about half way between the high voltage and a low voltage (such as GND), as is well known to those of ordinary skill in the art. By this means the capacitor circuit can sustain a voltage that is twice the oxide breakdown voltage of individual MOSFETs M1 and M2.

[0024] FIG. 8 shows side-elevational cross-sectional views of a PIP (poly-insulator-poly) capacitor 52 and a MIM (metal-insulator-metal) capacitor 53. In addition to polysilicon or metal, the conductors can be fabricated from any suitable conducting material as known to those of ordinary skill in the art.

[0025] FIG. 9 is a top view of a fringe capacitor 54. The capacitance derives from fringing in interleaved conductors. In addition to polysilicon or metal, the conductors can be fabricated from any suitable conducting material as known to those of ordinary skill in the art.

[0026] FIG. 10 is an electrical schematic diagram of two possible implementations 62, 64 of the diodes featured in the switch circuits of FIGS. 3, 4, 5, 6, 14A, 14B, 15, 16

and 17. The diodes may be realized by a diode-connected NMOS transistor 63 or a diode-connected PMOS transistor 64.

[0027] FIG. 11 is a side elevational cross-sectional diagram illustrating an implementation of a PN diode 66 (p+ (68) to n- well (26)) as may be used to implement the diodes featured in the switch circuits of FIGS. 3, 4, 5, 6, 14A, 14B, 15, 16 and 17.

[0028] FIG. 12 illustrates an electrical schematic diagram of an alternative circuit implementation 70 of a high-voltage nFET, that can be used as a replacement for any or all of the high-voltage nFETs in the switch circuits of FIGS. 3, 4, 5, 6, 13, 14A, 14B, 15, 16, 17 and 18. This alternative circuit configuration 70 uses a high-voltage nFET 72 as a cascode with its gate 74 connected to a bias voltage or to Vdd, and a second low-voltage nFET 76 to perform the switching operation in response to logic input "LI". Due to the cascode, the high-voltage nFET 72 in this alternative circuit configuration has a smaller maximum drain-to-gate voltage than in the configurations shown in the switch circuits of FIGS. 3, 4, 5, and 6 because its gate is pinned at Vdd rather than switching between ground and Vdd, so its gate oxide is less likely to break down under high drain voltages, resulting in less device stress and improved reliability.

[0029] FIG. 13 is an electrical schematic diagram of a fifth modification of the switch circuit of FIG. 1 in accordance with another embodiment of the present invention. In this embodiment, a switch circuit 78 provides a switched high-voltage output signal Vout in response to a complementary input logic-level state (Reset, Set, respectively) at nodes 80,

82. The nFET N5 is disposed between the source of nFET N4 and ground 84 and is biased by bias voltage source Bias2. A high-voltage nFET N2 is disposed between the drain of nFET N4 and control node 14. The pFET 86 is configured as a diode D2 with gate and drain coupled to control node 14, well coupled to a high-voltage supply HV, and source coupled to Intermediate-Voltage IV1. The pFET P1 is configured with its source and well coupled to the high-voltage supply HV, its gate coupled to Bias1 (a bias voltage set below HV), and its drain coupled to control node 14. The pFET P2 is configured with its source and well coupled to the high-voltage supply HV, its gate coupled to control node 14, and its drain coupled to intermediate node IN. A diode-connected pFET 88 is configured with its gate, drain and well coupled to intermediate node IN and its source coupled to Intermediate-Voltage IV2. The pFET P3 is coupled between intermediate node IN and output voltage node Vout with its gate coupled to intermediate voltage IV2, its source and well coupled to node IN, and its drain coupled to node Vout. High voltage nFET N1 is configured with its drain coupled to node Vout, its source coupled to the drain of nFET N3, and its gate coupled to Vdd. The nFET N3 has its source coupled to GND (ground) 84 and its gate coupled to Set logic input node 82. In accordance with this embodiment, the following voltages may be used: HV = 10V, Bias1 = 9.3V, IV1 = 6V, Vdd = 3.3V, Bias2 = 1V and IV2 = 6V. In this circuit note that the current drawn by nFET N5 is larger that the current sourced by the pFET P1, so when Reset node 80 is high, control node 14 pulls down until diode D2 turns on clamping control node 14 at IV1 less the voltage drop across diode D2. If Reset is low and Set if high, then transistor N4 is off and control node 14 goes high to HV, similarly transistor N3 is on and Vout goes low.

[0030] FIG. 14A is an electrical schematic diagram of a sixth modification 90 of the switch circuit of FIG. 1 in accordance with another embodiment of the present invention. In accordance with this embodiment of the invention, the switch circuit 90 provides a switched complementary high-voltage output signal Vout in response to two complementary input logic-level states on nodes 92 (Set) and 94 (Reset) and includes: a first and a second pFET P1, P2 having cross-coupled gates and drains with sources both coupled to a high-voltage supply node; a first and a second diode D1, D2 having their anodes coupled to an Intermediate-Voltage node 96 supplied with Intermediate-Voltage IV and their respective cathodes coupled to the respective drains of said first and second pFETs P1, P2; a third and a fourth pFET P3, P4 having their gates both coupled to said intermediate voltage node 96, their respective drains coupled to respective first and second complementary output voltage nodes 98, 100, and their respective sources coupled to said respective drains of said first and second pFETs P1, P2; a first and a second high-voltage nFET N1, N2 having their gates coupled to Vdd at Vdd supply node 101, their respective sources coupled to the drains of respective nFETs N3, N4, and their respective drains coupled to the respective complementary output voltage nodes 98, 100. The nFETs N3, N4 are configured with their sources coupled to GND 84, gates coupled to Reset and Set nodes 94, 92 (respectively), and drains coupled to the sources of HV nFETs N1, N2 (respectively). In this circuit, High-Voltage HV may be about 10V, Intermediate-Voltage IV may be about 6V, and Vdd may be about 3.3V in accordance with one embodiment. In another embodiment, there may be a pair of different intermediate voltages and node 96 may be divided into nodes 96a and 96b which are not

connected to one another, with one intermediate voltage being supplied to node 96a and another to node 96b. The diodes D1, D2 may be fabricated from diode-connected FETs such as pFETs in an nWell. Note that this circuit consumes zero static power in either the on state or the off state and does not require external bias voltages.

[0031] FIG. 14B is an electrical schematic diagram of a modification 102 of the circuit 90 illustrated in FIG. 14A and discussed in detail above. In the circuit 102 of FIG. 14B, diodes D3 and D4 are represented as diode coupled nFETs with their anodes coupled to Vdd and their cathodes coupled, respectively, to the source of high-voltage transistor N1 and drain of nFET N3 and to the source of high-voltage transistor N2 and drain of nFET N4. The diodes D3 and D4 could be fabricated in any conventional manner and this circuit also consumes zero static power in either the on state or the off state and does not require external bias voltages.

[0032] FIG. 15 is an electrical schematic diagram of a seventh modification 104 of the switch circuit of FIG. 1 in accordance with another embodiment of the present invention. In accordance with this embodiment of the invention, the switch circuit 104 provides a complementary switched high-voltage output signal Vout, in response to two complementary input logic-level states on nodes 92 (Set) and 94 (Reset) and includes: a first and a second pFET P1, P2 having cross-coupled gates and drains with sources both coupled to a high-voltage (HV) supply node 106; a first and a second diode D1, D2 having their anodes coupled to a first Intermediate-Voltage (IV-HIGH) node 108 and their respective cathodes coupled to the respective drains of said first and second pFETs

P1, P2; a third and a fourth pFET P3, P4 having their gates both coupled to said first Intermediate-Voltage node 108, their respective sources coupled to the respective drains of pFETs P1, P2, their respective drains coupled to respective sources of fifth and sixth pFETs P5, P6, gates of said fifth and sixth pFETs P5, P6 respectively coupled to a second Intermediate-Voltage (IV-LOW) node 110, a third and a fourth diode D3, D4 having their anodes coupled to the second Intermediate-Voltage node 110 and their respective cathodes coupled respectively to the drains of said third and fourth pFETs P3, P4; the drains of said fifth and sixth pFETs P5, P6 coupled respectively to complementary output voltage nodes 98, 100; a first and a second high-voltage nFET N1, N2 having both of their gates coupled to Vdd at Vdd supply node 101, their respective sources coupled to the drains of nFETs N3, N4, and their respective drains coupled to the respective complementary output voltage nodes 98, 100. The nFETs N3, N4 are configured with their sources coupled to GND 84, gates coupled to complementary logic input nodes Set (92) and Reset (94) (respectively) and drains coupled to sources of HV nFETs N1, N2 (respectively). In this circuit, the High-Voltage HV may be about 11V, Intermediate-Voltage-High (IV-HIGH) may be about 8.5V and Intermediate-Voltage-Low (IV-LOW) may be about 6V with Vdd about 3.3V in accordance with one embodiment of the present invention. This version uses two cascode stages 112, 114 (double cascode) to reduce the stress on the cascode pFET transistors with respect to the versions of FIGS. 14A and 14B. This technique may also be applied to the circuits of FIGS. 3, 4, 5, 6, 13 and 14. The diodes D1, D2, D3 and D4 may be fabricated from diode-connected FETs such as pFETs in an n- well or otherwise as will now be apparent to those of ordinary skill in the art.

[0033] FIG. 16 is an electrical schematic diagram of an eighth modification 116 of the switch circuit of FIG. 1 in accordance with another embodiment of the present invention, illustrating an alternative circuit implementation of a high-voltage latch. This alternative circuit configuration uses a second set of cascode devices (P3 and P4) to reduce the parasitic capacitance at drain nodes ("A" and "B") of the latching pFET pair (P1 and P2) to GND. Reducing the capacitance of nodes A & B to GND prevents both of the latching pFET transistors (P1 and P2) from turning on simultaneously, due to capacitive voltage division from the gate nodes of P1 and P2 to GND, when ramping up the high-voltage. In many cases, the high-voltage is generated by a high-impedance power supply which cannot handle the resulting current draw that occurs when both P1 and P2 are conducting simultaneously. By tying the n- well connections of P3 and P4 to the high-voltage node 106, the capacitance of nodes A and B are reduced when compared with the previously described HV switches. Small (low capacitance) n- well diodes DN1 and DN2, with their cathodes tied to nodes A and B and their anodes tied to GND, clamp the drain nodes of P1 and P2 to one diode voltage drop below GND when the high-voltage input node 106 is driven toward GND. These diodes are typically formed as shown in FIG. 11, but may be formed from diode-connected FETs such as pFETs in n-wells and the like. This approach of clamping nodes A and B to a diode below GND, and therefore to about the same voltage, discharges the cross-coupled pair (P1, P2) and thereby prevents the circuit from developing a "memory" for the previously latched state. It also prevents nodes A and B from reaching approximately -6V. In one embodiment of this circuit, the High-Voltage HV may be about 10V, the Intermediate-Voltage IV may

be about 6V, and Vdd may be about 3.3V. This double-cascode design uses a single Intermediate-Voltage (IV) applied at node 96. It consumes zero static power in the on state and in the off state.

[0034] FIG. 17 is an electrical schematic diagram of a ninth modification 118 of the switch circuit of FIG. 1 in accordance with another embodiment of the present invention, illustrating an alternative circuit implementation of a high-voltage latch. This alternative circuit configuration connects the anodes of diodes D1 and D2 to the Intermediate-Voltage node 98 rather than to GND (compare with circuit 116 in FIG. 16), to reduce the maximum Vds across transistors P1 or P2 when Vout on node 98 or its complement on node 100 are driven to GND, respectively. Small (low capacitance) n-well diodes, with their cathodes tied to nodes A and B and their anodes tied to the Intermediate-Voltage (IV) node 96, clamp the drain nodes of P1 and P2 to one Vf below IV when the High-Voltage (HV) input node 106 is driven toward GND. These diodes D1 and D2 are typically formed as shown in FIG. 11, but may be formed from diode-connected FETs such as pFETs in n- well, or the like. In one embodiment of this circuit, the High-Voltage HV may be about 10V, the Intermediate-Voltage IV may be about 6V, and Vdd may be about 3.3V. This double-cascode design uses a single Intermediate-Voltage. It consumes zero static power in the on state and in the off state.

[0035] The version of the circuit shown in FIG. 14A lacks the transistors labeled in FIG. 16 as P3 and P4. Accordingly, without these two transistors, the n- well capacitance of the pFET switches (P3, P4 in FIG. 14A and P5, P6 in FIG. 16) is located

at nodes A and B (drains of P1, P2, respectively). When the High-Voltage supply is stepped from 0 to about 10 Volts DC, this n- well capacitance shares charge with the gate capacitance of transistors P1 and P2. This can cause both P1 and P2 to turn on and can, under certain circumstances, prevent the high-voltage switch circuit from latching correctly.

[0036] Adding transistors P3 and P4 in FIG. 16 solved this n- well capacitance charge sharing issue because the n- wells of P3 and P4 (FIG. 16) are coupled to the High-Voltage supply. However, without the parasitic n- well diodes on nodes A and B illustrated in FIG. 16, these nodes may not discharge completely when the High-Voltage supply is stepped back down to GND. One of these nodes, depending upon which side of the switch was turned on, goes below GND when the High-Voltage supply goes low. This can result in a sometimes undesired memory of the last switch state and can make it difficult to change the state of the switch. Accordingly, the small n- well diodes DN1 and DN2 with their anodes coupled to GND and their cathodes coupled to node A and node B, respectively, solve this issue by clamping nodes A and B to GND.

[0037] Although the n-well diodes DN1 and DN2 in FIG. 16 are smaller than the PMOS n- wells discussed above, they can still cause enough charge sharing on nodes A and B of the FIG. 16 embodiment to raise issues. For example, with a 1.4 micron n- well diode, there is insufficient added capacitance to be a problem. However, with larger structures, such as a 3.0 micron n- well diode the capacitance increases to the point that it

can be an issue. This potential problem can also be obviated by the approach illustrated in FIG. 18, discussed below.

[0038] In the circuit shown in FIG. 17, diodes D1 and D2 serve to provide a discharge path for nodes A and B. Holding the anodes of D1 and D2 at IV instead of GND eliminates some of the capacitance otherwise present. Using MOS diodes (shorted MOSFETs) instead of n- well diodes also offers the opportunity to make much smaller structures with much smaller capacitances than using n- well diodes.

[0039] FIG. 18 is an electrical schematic diagram of a tenth modification 120 of the switch circuit of FIG. 1 in accordance with yet another embodiment of the present invention, illustrating an alternative circuit implementation of a high-voltage latch. Note that intermediate nodes A (IN1) and B (IN2) are clamped by n-well diodes DN1 and DN2, respectively, as described above in connection with the FIG. 16 embodiment. This alternative circuit uses a Preset input along with the Set and Reset inputs at nFETs N7 and N8 to "preset" or "precharge" one of the drain nodes (A or B) of the latching pFET pair (P1 and P2) before the High-Voltage supply coupled to HV node 106 is ramped high. Isolation from the high-voltages present in the switch circuit is provided by series connected (cascoded) high-voltage nFETs N5 and N6, respectively, which are left in the on state by applying Vdd to their gates. Presetting one of intermediate nodes A (IN1) or B (IN2) prevents both P1 and P2 from turning on simultaneously, due to capacitive voltage division from their gate nodes to GND, when ramping the High-Voltage supply. In many cases, the High-Voltage is generated by a high-impedance power supply which

cannot handle the resulting current draw that occurs when both P1 and P2 are conducting simultaneously. In this circuit, the High-Voltage HV may be about 10V, the Intermediate-Voltage IV may be about 6V, and Vdd may be about 3.3V. The circuit consumes zero static power in either the on state or the off state. Note that in the claims where a circuit element is referred to as being “responsive” to a logic level signal such as Reset, it is intended to include as well the situation where the circuit element is in fact responsive to the inverse or complement of the same signal, as, for example, the situation where an nFET responsive to Reset is replaced with a pFET which would have to be responsive to the complement of Reset (Set) in order to perform the same function.

[0040] As is now apparent, diode-transistor pairs (D1 and P3 in FIG. 3, but present in all circuits of the invention) are a key aspect in several embodiments of the present invention. For example, looking at FIG. 14A, when Vout on node 98 is low, the diode-transistor pair D1-P3 ensures that none of the series pFETs (P1 & P3) have excessive drain-to-source voltage across them. In FIG. 15 this idea is expanded upon by using two diode-transistor pairs in series (D1-P3 and D3-P5 on the left side of the circuit and D2-P4 and D4-P6 on the right side of the circuit) to further reduce the voltage stress on the three series pFETs (P1-P3-P5 on the left and P2-P4-P6 on the right).

[0041] Finally, those of ordinary skill in the art will now realize that CMOS silicon-on-sapphire (SOS) and silicon-on-insulator (SOI) technologies may also be used to fabricate the high-voltage switches as contemplated herein. Both of these technologies use insulating substrate materials for isolating individual devices. In these approaches, an

insulating material, typically silicon dioxide, is placed over the substrate material (either sapphire in SOS or silicon in SOI, and potentially other materials as will be apparent to those of ordinary skill in the art). A thin silicon layer is then placed on top of the oxide. Transistors are then fabricated in a similar fashion to bulk CMOS processes. Floating-gate devices may be used in these processes as well.

[0042] While embodiments and applications of this invention have been shown and described, it would be apparent to those skilled in the art having the benefit of this disclosure that many more modifications than mentioned above are possible without departing from the inventive concepts herein. For example, it is to be noted that while the present invention may be implemented in a single-well single-poly process and will work with various logic voltage levels from less than 1 Volt to greater than 10 Volts, the invention is not so limited and can be implemented in processes that support multiple polysilicon layers, multiple wells, and/or higher voltage devices. Furthermore, the concept of a high-voltage nFET as used herein is intended to encompass not only n-well devices, but also NLDD (N-type Lightly Doped Drain) devices and other lightly doped, or isolated structures that increase the reliable drain-to-gate and drain-to-source voltages of the device so that it, in effect, behaves like an LDMOS or DEMOS nFET in this respect. Finally, those of ordinary skill in the art will now recognize that MOS gates may be fabricated in a number of ways other than by heavily doped polycrystalline silicon. For example, they may be fabricated of metal or other conductors. The invention, therefore, is not to be restricted except in the spirit of the appended claims.